REMARKS

In this Amendment, Applicant has cancelled Claim 21 without prejudice or disclaimer, amended Claims 3, 4, 22, 27 and 28, and added new Claims 31 – 32 to overcome the rejections and specify the embodiments of the present invention. It is respectfully submitted that no new matter has been introduced by the amendment. All claims are now present for examination and favorable reconsideration is respectfully requested in view of the preceding amendments and the following comments.

OBJECTION TO CLAIM:

Claims 3 and 4 have been objected to because of certain informalities. It is respectfully submitted that the amended Claims 3 and 4 have corrected the informalities indicated by the Examiner. Therefore, withdrawal of the objection is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 102:

Claims 3, 4, 21 and 22 have been rejected under 35 U.S.C. § 102 (b) as allegedly being anticipated by Xilinx-E. Claims 3, 4, 21, 22, 27 and 28 have been rejected under 35 U.S.C. § 102 (b) as allegedly being anticipated by New wt al. (US 6,091,263).

Applicant traverses the rejection and respectfully submits that the present-claimed invention is not anticipated by the cited references. More specifically, the Examiner has stated, with reference to Claims 3, 4, 21, and 22, that the Virtex-E product specification "...discloses an FPGA in which a monitoring device may be connected via said means of access to said state data storage units, and said means of access to said state data storage units enables said monitoring device to read data values from said state data storage units and to write data values to said state data storage units while the user program continues to perform control functions...".

Applicant has amended Claims 3, 4, 22 and deleted Claim 21. Amended Claim 3 requires "... a dual purpose flip-flop for storing state data in said user program circuit, said dual purpose flip-flops, when connected in said user program circuit, are selectively

operable in a first way as a shift chain operable to provide both read and write access to said state data or in a second way as logic elements of said user program circuit...". The dual purpose flip-flop provides 'means as access' previously claimed.

The use of dual-purpose flip-flops facilitates the necessary speed of reaction required to produce correct output signals in response to input signals in a sufficiently timely manner so as to accommodate the control requirements of the machine/process. Their use does so by minimizing the time required to access user program circuit state data. The amended Claim 3 is therefore novel and not anticipated by the Virtex-E preliminary product specification.

The Examiner has stated, with reference to Claim 4, that "Virtex-E discloses a logic processing interval in sequence with a data access interval." Amended claim 4 requires:

- a logic processing mode in which said dual purpose flip-flops are operated as said logic elements in said user program circuit, and in which the clock to said dual purpose flip-flops is enabled, or
- a pause mode in which the clock to said dual purpose flip-flops is disabled.

The Virtex-E product specification does not disclose the use of dual-purpose flips-flops that enable a logic processing mode, a pause mode and a data access mode as required by amended Claim 4. Amended Claim 4 and subsequent dependent Claims 31, 27, 28, 32 and 33 are therefore novel and not anticipated by the Virtex-E product specification.

The examiner has further stated, with reference to Claims 21 and 22, that "Virtex-E discloses reading back the contents of the flip-flops to observe the internal logic state." Claim 21 has been deleted and Claim 22 has been amended to include additional features not disclosed by the reference.

As previously stated, amended Claim 3 requires a dual purpose flip-flop. Applicant is not aware of a previous instance of dual purpose flip-flops being used both

as operational parts in a digital circuit, and also for providing external access to read circuit state data, the two functions being multiplexed in such a way as to maintain control of an item under control while at the same time allowing access to the state data.

The Virtex-E product specification does not describe reading back the contents of the flip-flops by the use of a dual purpose flip-flop as required by the amended claims. The amended claims are therefore novel and not anticipated by the Virtex-E product specification. In addition, the following example is provided to illustrate the shortcomings of the Virtex-E.

The slow speed with which state data can be read and written with the Virtex-E is a serious disadvantage when the system is also required to maintain control of a machine or process because it directly increases the maximum time taken for outputs to respond to inputs. The Virtex-E state data access system is slow because it requires the transport of the user circuit state data dispersed within a large volume of configuration data.

By way of example, in an FPGA such as the Xilinx Virtex-E mid-sized XCV600E device, there are somewhat less than 15,000 flip-flops that are used for storing state data - the remainder are used for configuration purposes or memory. The configurable logic block read-back pattern for the XCV600E is 3,585,600 bits long. This is 239 times as long as the bitstream of interest of under 15,000 bits. And the bits of interest in the Virtex-E bitstream are not conveniently located but are dispersed throughout the whole configuration bit stream. Reading the circuit state via a configurable logic block read-back pattern at 60MHz takes 60ms. In contrast, the system according to the present invention would take only 250 microseconds.

The Examiner has stated that New et al. "...discloses an FPGA in which a monitoring device may be connected to via said means of access to said state data storage units, and said means of access to said state data storage units enables said monitoring device to read and write data values to said data storage units while the user control program continues to perform control functions."

Applicant has amended Claims 3, 4, 22, 27 and 28. Claim 21 has been deleted. In addition, the applicant provides the following comments:

The amended Claim 3 requires a dual purpose flip-flop configured into the programmable logic hardware to provide the access to state data. New et al does not disclose dual purpose flip-flops as claimed in amended Claim 3.

The applicant is unaware of any previous disclosure of dual-purpose flip-flops as claimed in amended claim 3, and believes for the reasons stated above that their use for both accessing and processing user circuit state data while maintaining control is an inventive and novel feature of their development. This is particularly so because of the benefits provided such as the ability to modify programs and resynchronise triple redundancy FPGA sets, both while maintaining control.

Regarding Claim 27, the word "corresponding" implies that the state data will be relocated as necessary to ensure that each bit of data written into the newly configured circuit is placed into the bit that provides the same circuit function as the bit in the circuit from which it was read. Claim 27 has therefore been amended for clarification. Claim 27 and 28 have also been amended to specifically cover embodiments that perform swaps in single sections of programmable logic hardware, and those that use two separate sections, swapping out of one section into the other, both embodiments being supported in the applicant's specification.

Therefore, the presented claims are not anticipated by Xilinx Virtex-E and New and the rejection under 35 U.S.C. § 102 (b) has been overcome. Accordingly, withdrawal of the rejections under 35 U.S.C. § 102 (b) is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 103:

Claims 27 – 28 have been rejected under 35 U.S.C. § 103 (a), as allegedly being obvious and unpatentable over Virtex-E in view of New.

Applicant traverses the rejection. It is respectfully submitted that the cited references fail to render the embodiments of the present invention as claim obvious. As explained above, the cited references are significantly different from the present invention as defined in the amended Claims 27 – 28. The differences between the embodiments of the present invention have been specified as above. There is no motivation to combine Virtex-E with New. Because the differences indicated above, even if they are combined, they will not render the embodiments of the present invention as amended obvious.

Therefore, the rejection under 35 U.S.C. § 103 has been overcome. Accordingly, withdrawal of the rejection under 35 U.S.C. § 103 is respectfully requested.

Having overcome all outstanding grounds of rejection, the application is now in condition for allowance, and prompt action toward that end is respectfully solicited.

Respectfully submitted,

JACOBSON HOLMAN PLLC

Date: March 6, 2008
(202) 638-6666
400 Seventh Street, N.W.
Washington, D.C. 20004
Atty. Dkt. No.: P67300US0

By _____
John C. Holman
Registration No. 22,769